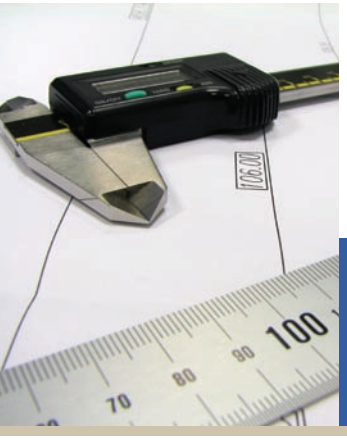

SDR applications: One size does not fit all

By Andrew Reddig

Engineers designing modern SDR applications know there are many trade-offs between options, including PMC/XMC versus VXS. As newer FPGA technology is developed and deployed, however, VXS will be better able to satisfy growing requirements for more board and front-panel space, higher densities, more IP core and I/O choices, and improved analog performance than PMCs or XMCs.

Many Software-Defined Radio (SDR) applications can be addressed efficiently and cost effectively within the constraints imposed by modular PMC- or XMC-based architectures (up to four coherent channels with good analog performance and limited FPGA density). However, some SDR applications require more board and front-panel space, higher functional density via FPGAs, more IP core and I/O options, and better analog performance, or some combination thereof. For those applications, it makes sense to look at using ANSI/VITA 41 (VXS) as an architecture that provides a more optimized implementation over a PMC- or XMC-based approach. Our discussion includes the review of a VXS-based SDR testbed (Figure 1) supporting two primary antenna inputs and a reference input, with I/Q sampling at 16-bit resolution, along with a coherent D/A output signal.

Space: The final frontier

The trade-off between PMC/XMC modules and VXS cards is fundamentally about space – board space for components and front-panel space for connections to the outside world.

Both the PMC and XMC standards are based on IEEE 1386, which defines a single-wide card as 74 mm x 149 mm with a 4.7 mm height constraint over most of the card. A relatively large portion of the card is reserved for connectors, particularly if the designer implements a combination module that has both the traditional PCI connectors and the new XMC switched fabric connector. The end result is that a modular I/O product is typically very space constrained relative to its required functionality. A typical high-density PMC or XMC module targeted at SDR applications provides four A/D inputs connected to an FPGA processor with one or two banks of onboard memory and a local bus or fabric interface. A PMC front panel is typically limited to the analog I/O connectors with little room leftover for network or other adjunct interfaces.

A VXS payload card, on the other hand, provides a much larger canvas to work with, measuring 160 mm x 233 mm with a height constraint of 13.7 mm. With 3.4x the raw area and 9.8x the volume compared to a PMC/XMC module, a VXS payload card supports larger FPGA devices, deeper memory buffers, and improved onboard and offboard connectivity options. The larger 6U x 4HP front panel provides room for additional connectors for direct attachment to network and storage interfaces.

To illustrate this, the SDR testbed uses a Quixilica Tarvos VXS card as the core acquisition and processing (A/P) card in the system. In a minimum configuration, the A/P card can simply be mounted in an enclosure with no backplane and a discrete power connection, which results in the smallest and lightest system. (For future expansion and laboratory convenience, the SDR testbed is built using a three-slot VXS chassis with an embedded SBC and a spare slot, as shown in Figure 2.) All of the control and monitoring functions performed by the SBC can also be performed on a stand-alone system using a laptop attached to the front-panel GbE port of the A/P card.

Higher-density FPGAs increase functionality options

The A/P card in the SDR testbed uses a Xilinx Virtex-II Pro V2P70 FPGA device in an FF1517 package, which has 40 percent more gates and 39 percent more I/O pins than the FPGA devices typically used on PMC and XMC modules. The additional gates allow for application-specific signal processing, additional network or storage functionality, or both, depending on the specific requirements implemented. The additional I/O pins, coupled with the additional board space in a VXS form factor, allow the A/P card to support four independent DDR memory

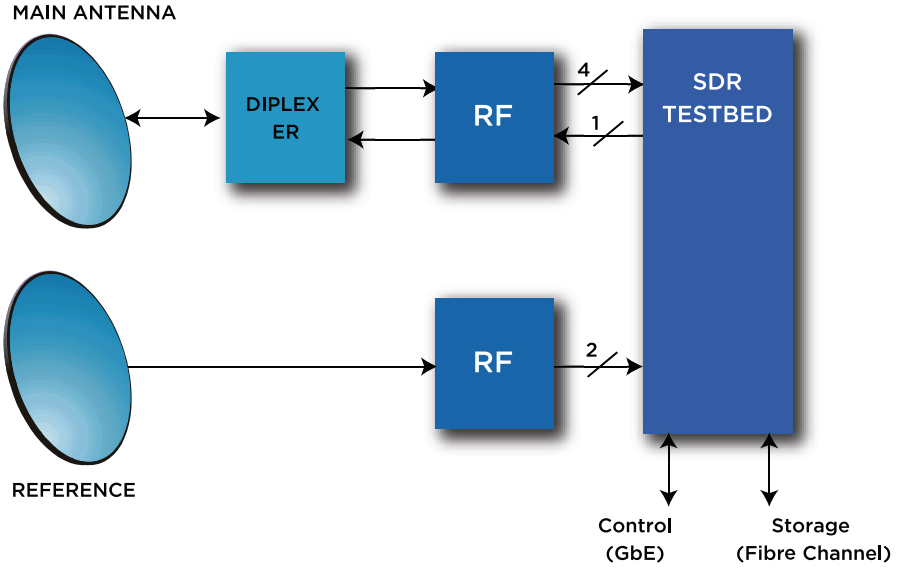

Figure 1

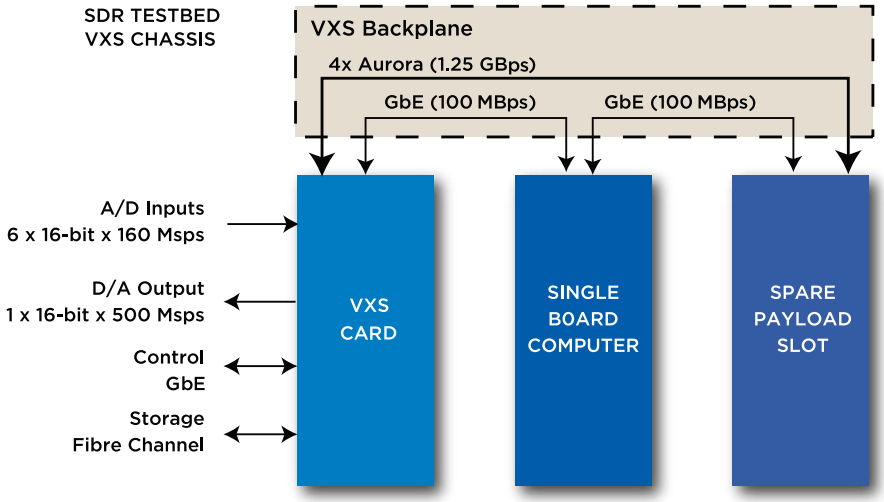

Figure 2

banks, supporting multiple simultaneous high-speed streaming interfaces within one FPGA device.

The FPGA is used to perform multiple functions depending on the specific algorithm exercised:

- Signal processing the input stream into one or more narrowband channels
- Retransmit of information based on the processed input stream combined with a waveform preloaded into memory from either the attached storage or through one of the GbE interfaces
- Snapshot capture of input streams into memory buffers that can be recorded to attached storage when triggered
- Output of control and status information and selected narrowband data to either an attached laptop or an embedded SBC through a GbE interface

By providing a high-density FPGA with multiple independent memory interfaces, a VXS-based implementation enables the development of the SDR testbed firmware without the need to split the functions across multiple cards or multiple devices.

Integrating IP and I/O

The VXS-based SDR testbed's firmware is built using a combination of off-the-shelf IP cores for utility functions such as I/O interfacing, networking, and storage, along with application-specific algorithms built on top of signal processing cores. While each individual function is relatively small, the whole SDR testbed application and the set of IP modules used to implement it requires FPGA density, memory bandwidth, and I/O capabilities that are not available within the constraints of PMC/XMC architectures.

While the VXS card provides the necessary gate density and I/O options, hardware capability utilization can only be accomplished by using IP cores that support the underlying hardware and make it accessible to the user's application. A diagram of the SDR testbed application with the associated internal IP cores is shown in Figure 3.

The utility cores used by the SDR testbed include:

- ***ADC interface –*** Abstracts the details of the A/D interface from the user's FPGA firmware and isolates the user application from the detailed design and timing constraints of the A/D interface circuitry.
- ***DAC interface –*** Abstracts the details of the D/A interface from the user's FPGA firmware.
- ***DDR interface –*** Allows the user application to read and write DDR SDRAM memory using a simple FIFO-based interface. DDR Bank #1 uses this core to allow the SDR application to use one DDR memory bank as a workspace.
- ***DDR controller –*** Supplied as a part of the JazzStore System-on-Chip (SoC) embedded recorder IP core.
- ***JazzStore SoC –*** Uses the embedded PPC405 PowerPC processor and one of the DDR memory banks to implement an embedded data recorder and playback application within the FPGA. The recorder accesses external storage using the Fibre Channel protocol through a front-panel Small Form-Factor Pluggable (SFP) fiber optic interface.

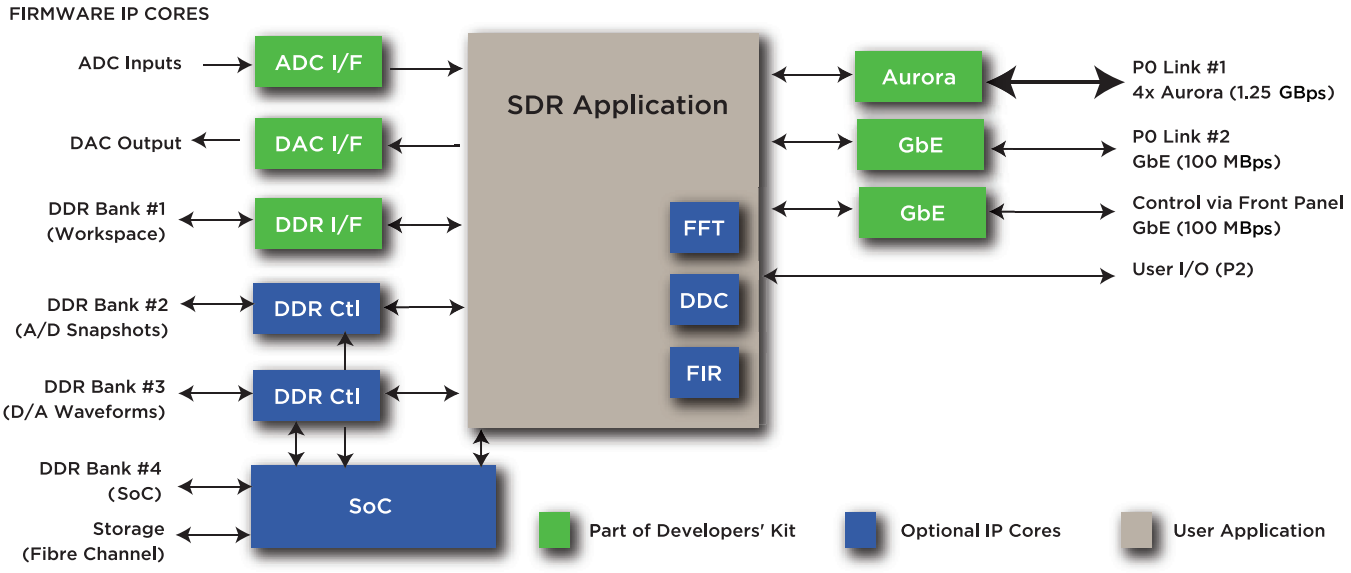

Figure 3

- ***GbE –*** Provides a UDP/IP interface between the SDR testbed user application and the P0 connector (used to communicate with the embedded SBC). A second instance of this IP core provides an equivalent interface to one of the two front-panel SFP interfaces.
- ***Xilinx Aurora –*** Provides a high-speed interface to the adjacent VXS payload slot through the P0 connector, enabling the SDR testbed user application to simultaneously send and receive data at up to 1.25 GBps.

In addition to the utility cores that are specific to the underlying hardware platform, the SDR testbed application can also utilize off-the-shelf signal processing cores from a wide range of sources for functions such as Fast Fourier Transforms (FFTs), Digital Down Converters (DDCs), and Finite Impulse Response digital filters (FIRs).

Keeping the noise down

Key performance requirements for any Software-Defined Radio system include the bandwidth, resolution, and noise performance of the analog inputs. Accordingly, two of the most important metrics of analog performance are *Signal-to-Noise Ratio*, or *SNR*, and *Spurious Free Dynamic Range*, or *SFDR*. Both SNR and SFDR are largely dependent on the design and layout of the A/D board, particularly the layout of the analog inputs, the separation of analog and digital signals, and the design and filtering of the analog power supplies. A VXS payload card design has several built-in advantages over PMC or XMC cards in these areas.

First and foremost, because a 6U VXS card is simply less space constrained than an I/O module, it enables the designer to maintain better physical and electrical isolation between the card's analog and digital regions. The larger card also allows for better power supply filtering and layout with fewer mechanical constraints than an I/O module.

In our VXS SDR testbed, the analog components are further isolated by being mounted on a physically separate mezzanine card. No digital components are located on the baseboard underneath the mezzanine card, and so the possibilities for crosstalk and interference effects are minimized. The end result is very high signal integrity in the analog domain, along with dense FPGA processing and memory resources in the digital domain.

While a PMC- or XMC-based solution also uses a mezzanine card, the trade-offs are significantly different. In the SDR testbed – which uses the Linear Technology LTC2209 A/D converter and provides 16-bit resolution at up to 160 Msps with 77 dB SNR and 100 dB SFDR – the mezzanine card is restricted to analog components only. Meanwhile, a PMC or XMC module will typically include FPGA, memory, power supply, and analog components all on the same card.

Also, the signal quality of the I/O module is driven somewhat by the layout and noise characteristics of the baseboard components located in close proximity to the analog portion of the I/O module. Because a PMC/XMC module and the associated baseboard are developed independently, usually by different vendors, the resulting combination is unlikely to reach peak performance.

More growth, fewer limitations

In today's SDR applications, there are trade-offs between alternatives such as PMC/XMC versus VXS. As newer FPGA technology is developed and deployed, VXS will be better able to satisfy growing requirements for more board and front-panel space, higher densities, more IP core and I/O choices, and improved analog performance than PMC/XMC alternatives. While PMC and XMC modules will also improve, the flexibility provided by a larger form factor such as VXS will become more critical as cards continue to push the limits of functional density. Hence, there will continue to be a need for a wide range of options to meet the needs of the SDR marketplace. **CS**

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